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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,796	07/10/2003	Timothy P. Gibson	H0004400	1971
128	7590	11/03/2006		EXAMINER
				VLAHOS, SOPHIA
			ART UNIT	PAPER NUMBER
				2611

DATE MAILED: 11/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

5P

Office Action Summary	Application No.	Applicant(s)
	10/616,796	GIBSON ET AL.
	Examiner	Art Unit
	SOPHIA VLAHOS	2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 10 July 2003.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-59 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-16, 18, 19, 21-54 and 56-59 is/are rejected.
 7) Claim(s) 17, 20 and 55 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 10 July 2003 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>12/12/05 3/7/05 2/28/05</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

1. Claim 18 is objected to because of the following informality: Claim 18 (line 6 after the preamble), recites: "...operable to receive said analog signals..." however line 3 after the preamble mentions "...an analog signal...". Correction or clarification is required.

Claim 53 contains a similar informality that should also be addressed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-16, 18-19, 21-45 are rejected under 35 U.S.C. 102(b) as being anticipated by Bexten (U.S. 6,205,133).

With respect to claim 1, Bexten discloses: a front-end circuit operable to receive a plurality of radio signals transmitted across a frequency band and generate an analog signal corresponding to a plurality of channels within said frequency band (see Fig. 5, combination of elements 205 (antenna), 505 (down-converter), 215 (LNA), 510 (BPF filter), comprise the front-end circuit, see column 4, lines 4-10, where components shown in Fig. 2 are also present in Fig. 5); an analog to digital converter coupled to said front-end circuit (Fig. 5, element 220, ADC), said analog to digital converter

operable to receive and convert said analog signal to a digital signal (Fig. 5, element 220, ADC); and a digital processing system coupled to said analog to digital converter (see Fig. 5, cascaded elements 315 ("Uplink Channel Selector"), 325 ("Multi-Channel Demodulator"), 330 ("Uplink Time Switch"), under the control of "resource manager" , see column 2, lines 56-58 where the system of Fig. 5 can be used in the hub station of Fig. 3, and see column 4, lines 43-47 for an example of the function of the hub station, (it delivers voice signals to MSC), said digital processing system operable to receive said digital signal and generate at least one output signal corresponding to at least one of said plurality of channels within said frequency band (see column 7, lines 1-2 , 26-32 , where the DSPs (elements 535 of Fig. 5) generate output signals corresponding to single carries that were included in the FDM wideband signal).

With respect to claim 2, all of the limitations of claim 2, are analyzed above in claim 1, and Bexten discloses: wherein said digital processing system generates a single output signal comprising a time-domain multiplexed serial data link (this is performed by element 330, "Time Switch" shown in Fig. 5, see column 7, lines 28-32).

With respect to claim 3, all of the limitations of claim 3, are analyzed above in claim 2, and Bexten discloses: further comprising a controller coupled to said digital processing system (see column 3, lines 6-7, the MSC (the mobile switching center) is considered as the controller receiving the time-domain multiplexed data via the T1 connection (see Fig. 3, output of block 350)), said controller operable to receive said time-domain multiplexed serial data link and generate a plurality of signals for

transmission to a plurality of end devices (see column 3, lines 8-11, where the “other communication networks” correspond to “the plurality of end devices”).

With respect to claim 4, all of the limitations of claim 4, are analyzed above in claim 1, and Bexten discloses: wherein said digital processing system generates a plurality of output signals comprising a plurality of signals for transmission to a plurality of end devices (see Fig. 5, where output T1 comprises (a plurality of) time domain multiplexed signals from the plurality of DSPs , and see column 4, lines 43-47, where during every uplink operation generates a signal T1 (comprising the time-domain multiplexed signals))

With respect to claim 5, all of the limitations of claim 5, are analyzed above in claim 1 (see antenna element “205” of Fig. 5).

With respect to claim 6, all of the limitations of claim 6, are analyzed above in claim 1 (see LNA element 215 of Fig. 5).

With respect to claim 7, all of the limitations of claim 7, are analyzed above in claim 1 (see band-pass filter element “510” of Fig. 5).

With respect to claim 8, all of the limitations of claim 8, are analyzed above in claim 7 (filter “510” is a band-pass filter).

With respect to claim 9, all of the limitations of claim 9, are analyzed above in claim 5, and Bexten discloses: wherein said front-end circuit further comprises an intermediate frequency mixing circuit operable to translate said received radio signals to an intermediate frequency band (Fig. 5, element 50 and LO input, see also, Fig. 2, LO and mixer 210, column 4, lines 9-10).

With respect to claim 10, all of the limitations of claim 10, are analyzed above in claim 1, and Bexten discloses: a digital down converter operable to select said at least one of said channels within said frequency band (see element(s) 520 "Digital Receiver" of Fig. 5, details of which are shown in Fig. 6, and column 7, lines 3-7); and a digital signal processor operable to extract information from said at least one of said channels and generate said at least one output signal (see Fig. 5, element 325 demodulator including elements 535, "DSP", column 7, lines 26-29 under the control of the "resource manager" also uses the RSSI level indicator to extract information from the channels and control the switch 530 that controls the inputs to the DSPs).

With respect to claim 11, all of the limitations of claim 11, are analyzed above in claim 10, and Bexten discloses: wherein said digital down converter selects said at least one of said channels according to configurable channel selection parameters (see column 7, lines 18-20, the digital receivers "520" are programmable to select and process any (frequency) channel also see column 1, lines 50-57, where programmable

frequency bandwidths are mentioned, and column 8, lines 5-8 where the programmable receivers can accommodate different standards (GSM, AMPS, DECT, etc)).

With respect to claim 12, all of the limitations of claim 12, are analyzed above in claim 11, and Bexten discloses: wherein said configurable channel selection parameters are software configurable (column 7, lines 18-20, where the "programmable" digital receivers is interpreted to correspond to "software configurable").

With respect to claim 13, all of the limitations of claim 13, are analyzed above in claim 11, and Bexten discloses: wherein said configurable channel selection parameters are selected from the group consisting of channel frequency, channel bandwidth, and combinations thereof (see column 7, lines 18-20, where it is mentioned that the digital receivers can be programmed to select any single channel within the FDM spectrum, and column 3, lines 18-23, where the FDM spectrum includes 416 (each one spans 30KHz), channels for a total of 12.5MHz, therefore to select any one of these 416 channels involves changing a channel (center) frequency, and also see column 1, lines 50-57, where programmable frequency bandwidths are mentioned, and column 8, lines 5-8 where the programmable receivers can accommodate different standards (GSM, AMPS, DECT, etc)).

With respect to claim 14, Bexten discloses: wherein said digital signal processor extracts said information from said at least one of said selected channels according to

configurable channel decoding parameters (see column 7, lines 38-46, where the number of diversity branches connected to a single DSP that demodulates (decodes) the channels, can be adjusted and also see column 7, lines 56-60 where the channel information format (voice or control signal) is determined).

With respect to claim 15, all of the limitations of claim 15 are analyzed above in claim 14, and Bexten discloses: wherein said configurable channel decoding parameters are software configurable (the resource manager couples the outputs out of element 530 to each DSP 535, see column 7, lines 23-25, and the resource manager can be software based, see column 5, lines 40-45).

With respect to claim 16, all of the limitations of claim 16, are analyzed above in claim 14, and Bexten discloses: wherein said configurable channel decoding parameters are selected from the group consisting of channel frequency, channel modulation scheme, channel bandwidth, channel information format, and combinations thereof (see channel information format, see column 7, lines 56-60 where the channel information format (voice or control signal) is determined).

With respect to claim 18, Bexten discloses: least one front-end circuit group comprising a plurality of front-end circuits (see Fig. 5, one out of the plurality of receiving branches, and the plurality of front-end circuits includes elements 205, 505, 215, 510), wherein each of said front-end circuits is operable to receive a plurality of radio signals

transmitted across a frequency band and generate an analog signal corresponding to a plurality of channels within said frequency band (see column 4, lines 4-10, where the antenna captures a wideband signal that includes a plurality of FDM channels, and notice that since elements 205, 505, 215 and 510 are cascaded, each one of them generates (outputs) an analog signal corresponding to a plurality of channels with said frequency band (the FDM carries)); at least one analog to digital converter coupled to said at least one front-end circuit group (see element 220 of Fig. 5 ADC of the first branch), said analog to digital converter operable to receive said analog signals from said front-end circuits (where it receives analog signal(s) corresponds to the analog signal supplied to ADC 220, that includes a plurality of analog carrier signals) and convert said analog signals to a digital signal (output of element ADC); and a digital processing system coupled to said at least one analog to digital converter (see Fig. 5, digital processing system includes blocks 315, 325, and 330, and "resource manager") said digital processing system operable to receive said digital signal from said analog to digital converter and generate at least one output signal corresponding to at least one of said channels within said frequency band of at least one of said front-end circuits (see column 7, lines 1-2 , 26-32 , where the DSPs (elements 535 of Fig. 5) generate output signals corresponding to single carries that were included in the FDM wideband signal).

With respect to claim 19, all of the limitations of claim 19 are analyzed above in claim 18, and Bexten discloses: wherein said digital processing system is operable to generate a plurality of output signals (see Fig. 5, where output T1 comprises (a plurality

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of) time domain multiplexed signals from the plurality of DSPs , and see column 4, lines 43-47, where during every uplink operation generates a signal T1 (comprising the time-domain multiplexed signals), wherein each of said output signals corresponds to at least one of said channels within said frequency band of at least one of said front-end circuits.

With respect to claims 21-27, these claims are analyzed similarly to claims 5, 6, 7, 10, 11, and 14 respectively.

With respect to claim 28, all of the limitations of claim 28, are analyzed above in claim 18, and Bexten discloses: comprising a plurality of front-end circuit groups and a plurality of corresponding analog to digital converters, wherein said digital processing system is operable to receive a plurality of digital signals from said analog to digital converters and generate at least one output signal corresponding to at least one of said channels within said frequency band of at least one of said front-end circuits of at least one of said front-end circuit groups (see Fig. 5, the plurality of front-end circuit groups correspond to the plurality of receiving branches, and DSPs 535 see column 7, lines 16-29, where the DSPs process channels extracted from the FDM spectrum by the digital receivers 520).

With respect to claim 29, Bexten discloses: a plurality of front-end circuits each of

which comprises an antenna circuit operable to receive a plurality of radio signals transmitted across a frequency band (see Fig. 5, plurality of receiving antennas and corresponding cascaded elements 505, 215, 510 and see column 4, lines 4-10), wherein each of said front end circuits is operable to generate an analog signal corresponding to a plurality of channels within said frequency band (column 4, lines 4-10; a plurality of analog to digital converters each of which is coupled to at least one of said front-end circuits, wherein each of said analog to digital converters is operable to receive said analog signal from said at least one of said front-end circuits and convert said analog signal to a digital signal; and a digital processing system coupled to each of said analog to digital converters, said digital processing system operable to receive said digital signals from said analog to digital converters and generate at least one output signal corresponding to at least one of said channels within said frequency band of at least one of said front-end circuits.

With respect to claims 30-32, the base limitations of these claims are analyzed above in claim 29, and these claims are analyzed similarly to claims 6-9 respectively.

With respect to claim 33, all of the limitations of claim 33, are analyzed above in claim 29 (where plurality of ADCs receive analog signals (from each receiving branch)).

With respect to method claims 34-40, these claims are analyzed similarly to apparatus claims 1, 6, 7, 9, 10, 2, and 4 respectively.

With respect to claim 41, all of the limitations of claim 41 are analyzed above in claim 34, and Bexten discloses: wherein a plurality of output signals are generated each of which corresponds to at least one of said digitized channels within said frequency band (see column 7, lines 26-32).

With respect to claim 42, all of the limitations of claim 42, are analyzed above in claim 41, and claim 42 is analyzed similarly to claim 4 above.

With respect to claims 43-45, these claims are analyzed similarly to claims 1, 2, and 4 respectively.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 4-7, 18-19, 21-24, 29-37, 43 are rejected under 35 U.S.C. 102(e) as being anticipated by Carlin et al., (U.S. 6,898,235).

With respect to claim 1, Carlin et al., disclose: a front-end circuit operable to receive a plurality of radio signals transmitted across a frequency band and generate an analog signal corresponding to a plurality of channels within said frequency band (see

Fig. 1a, combination of elements 5 (receiving antenna) and element 10, "RCVR module" that includes wideband (WB) receiver 110, column 9, lines 65-67, column 10, lines 1-6 , where the wideband receiver can captures signals for example in the VHF, UHF bands (mentioned in lines 10-14 of column 10); an analog to digital converter coupled to said front-end circuit, said analog to digital converter operable to receive and convert said analog signal to a digital signal (Fig. 1, element 210 ADC, column 10, lines 17-19); and a digital processing system coupled to said analog to digital converter (see Fig. 1a, components receiving the outputs of ADC element 210, including "Signal Processor Module" element 40 and its outputs), said digital processing system operable to receive said digital signal and generate at least one output signal corresponding to at least one of said plurality of channels within said frequency band (Fig. 1a, outputs of "Channel Processor" elements within the "Signal Processor Module" element 40 and Fig. 4 shows details of the "Channel Processor" element, that includes "demodulation/ recognition processors" and see column 22, lines 4-15, where includes "demodulation/ recognition processors" perform signal identification, and column 21, lines 59-62, mention an FSK signal as an example).

With respect to claim 4, all of the limitations of claim 4 are analyzed above in claim 1, and Carlin et. al., disclose: wherein said digital processing system generates a +plurality of output signals comprising a plurality of signals for transmission to a plurality of end devices (see column 18, lines 18-22, where high-speed data (see all outputs out of "Channel Processors" shown in Fig. 1a and see that the data on bus 83 of Fig. 1a is

supplied to the digital recoding means 90 as shown in Fig. 1a and for example to a display device (as mentioned in column 18, lines 18-22)).

With respect to claim 5, all of the limitations of claim 5 are analyzed above in claim 1, and Carlin et al., disclose: wherein said front-end circuit comprises an antenna circuit operable to receive said radio signals (see receiving antenna of Fig.5).

With respect to claim 6, all of the limitations of claim 6, are analyzed above in claim 5, and Carlin et al., disclose: wherein said front-end receiver further comprises an amplifier circuit operable to amplify said received radio signals (as part of the wideband receiver 110, see column 10, lines 2-3).

With respect to claim 7, all of the limitations of claim 5 are analyzed above in claim 5, and Carlin et al., disclose: wherein said front-end circuit further comprises a filter circuit operable to filter said received radio signals (see column 10, lines 1-2, the analog filtering circuitry).

With respect to claim 18, Carlin et. al., disclose: at least one front-end circuit group comprising a plurality of front-end circuits (see embodiment shown in Fig. 1b), wherein each of said front-end circuits is operable to receive a plurality of radio signals transmitted across a frequency band and generate an analog signal corresponding to a plurality of channels within said frequency band (where the front-end circuits include the receiving antenna and "WB Rcvr" of each branch, column 9, lines 65-67, column 10,

lines 1-6 , where the wideband receiver can captures signals for example in the VHF, UHF bands (mentioned in lines 10-14 of column 10); at least one analog to digital converter coupled to said at least one front-end circuit group (see ADC 210 of Fig. 1b), said analog to digital converter operable to receive said analog signals from said front-end circuits and convert said analog signals to a digital signal (ADC 210 receives the analog signal out of wideband receiver that includes a plurality of analog carrier signals); and a digital processing system coupled to said at least one analog to digital converter, said digital processing system operable to receive said digital signal from said analog to digital converter and generate at least one output signal corresponding to at least one of said channels within said frequency band of at least one of said front-end circuits ((Fig. 1b, outputs of "Channel Processor" elements within the "Signal Processor Module" element 40 and Fig. 4 shows details of the "Channel Processor" element, that includes "demodulation/ recognition processors" and see column 22, lines 4-15, where includes "demodulation/ recognition processors" perform signal identification, and column 21, lines 59-62, mention an FSK signal as an example)

With respect to claims 19, 21-24, all of the base limitations of these claims are analyzed above in claim 18, and these claims are rejected similarly to claims 4, 5, 6, 7, and 9 above.

With respect to claims 29, Carlin et al, disclose: a plurality of front-end circuits each of which comprises an antenna circuit operable to receive a plurality of radio signals

transmitted across a frequency band, wherein each of said front end circuits is operable to generate an analog signal corresponding to a plurality of channels within said frequency band (see each one of the receiving branches shown in Fig. 1b, ,see also column 9, lines 65-67, column 10, lines 1-6 , where the wideband receiver can captures signals for example in the VHF, UHF bands (mentioned in lines 10-14 of column 10); a plurality of analog to digital converters each of which is coupled to at least one of said front-end circuits, wherein each of said analog to digital converters is operable to receive said analog signal from said at least one of said front-end circuits and convert said analog signal to a digital signal (see each one of the ADC 210...210' of Fig. 1b); and a digital processing system coupled to each of said analog to digital converters, said digital processing system operable to receive said digital signals from said analog to digital converters and generate at least one output signal corresponding to at least one of said channels within said frequency band of at least one of said front-end circuits (((Fig. 1b, outputs of "Channel Processor" elements within the "Signal Processor Module" element 40 and Fig. 4 shows details of the "Channel Processor" element, that includes "demodulation/ recognition processors" and see column 22, lines 4-15, where includes "demodulation/ recognition processors" perform signal identification, and column 21, lines 59-62, mention an FSK signal as an example).

With respect to claims 30-33, all of the base limitations of these claims are analyzed above in claim 29, and these claims are rejected similarly to claims 6, 7, 9, and 29 respectively.

With respect to method claims 34-37 these claims are analyzed similarly to apparatus claims 1, 6, 7, and 9 respectively.

Claim 43 is analyzed similarly to claim 1 above.

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

7. Claims 1, 5-7, 9, 34-37, 43 are rejected under 35 U.S.C. 102(a) as being anticipated by Allpress et al. (U.S. 6,496,546).

With respect to claim 1, Allpress et al., disclose: a front-end circuit operable to receive a plurality of radio signals transmitted across a frequency band (see Fig. 4, receiving antenna element 208, and “RF-TO-IF CONVERTER” element 401 part of receiver 301, see column 4, lines 16-24, 59-65 see received “wide-band” signals containing plurality of narrowband signals (carriers)) and generate an analog signal corresponding to a plurality of channels within said frequency band (see column 4, lines 59-63, analog IF signal out of element 401); an analog to digital converter coupled to said front-end circuit, said analog to digital converter operable to receive and convert said analog signal to a digital signal (see Fig. 4, “A/D Converter” element 402, see column 5, lines 5-10, for a TDMA system, and column 4, lines 25-29, where 15MHz is the

wide-band signal received and it contains 500 carriers (narrowband signals)); and a digital processing system coupled to said analog to digital converter (see Fig. 4, elements 403-407, and controller 303-R are considered to comprise the digital signal processing system) said digital processing system operable to receive said digital signal and generate at least one output signal corresponding to at least one of said plurality of channels within said frequency band (see Figures 5, (and Fig. 6 for details on step 512), step 515 performed by the demodulator 407 of Fig. 4, see demodulation of M narrow-band uplink channels, column 8, lines 17-19).

With respect to claim 5, all of the limitations of claim 5 are analyzed above in claim 1, and Allpress et al., disclose: wherein said front-end circuit comprises an antenna circuit operable to receive said radio signals (see Fig. 4 antenna element 208, column 4, line 16).

With respect to claim 6, all of the limitations of claim 6, are analyzed above in claim 1, and Allpress et. al., disclose: wherein said front-end receiver further comprises an amplifier circuit operable to amplify said received radio signals (column 4, lines 59-60).

With respect to claim 7, all of the limitations of claim 7, are analyzed above in claim 6, and Allpress et. al., disclose: wherein said front-end circuit further comprises a filter circuit operable to filter said received radio signals (see column 4, lines

With respect to claim 9, all of the limitations of claim 9, are analyzed above in claim 5, and Allpress et al., disclose: wherein said front-end circuit further comprises an intermediate frequency mixing circuit operable to translate said received radio signals to an intermediate frequency band (see Fig. 4, element 410, "RF-TO-IF Converter", column 4, lines 59-62).

With respect to method claims 34-37, these claims are analyzed similarly to claims 1, 6,7, and 9 above.

With respect to claim 43, claim 43 is analyzed similarly to claim 1 above.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 46-54, 56-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bexten(U.S. 6,205,133) in view of Mano (U.S. 6,816,715).

With respect to claim 46, claim 46 is analyzed similarly to claim 1 (see 102(b) rejection under Bexten) but Bexten does not teach: wherein said frequency band

comprises aviation-band radio signals. In the same field of endeavor, Mano discloses: a frequency band comprises aviation-band radio signals (see

At the time of the invention, it would have been obvious to a person skilled in the art to configure the wideband receiver of Bexten et. al., to receive over a frequency band that comprises aviation-band radio signals (see column 1, lines 55-58, aeronautical radio spans 108MHz – 136MHz with a channel width of 25kHz). to provide a intelligent wideband receiver that centralizes, re-uses and shares system resources (see column 1, lines 50-55 of Bexten) for processing airline/aviation signals.

With respect to claims 47, 48, all of the limitations of these claims are analyzed above in Claim 46, but it is not taught that the aviation-band signals comprise aviation navigation radio signals (claim 47) and aviation communication radio signals (claim 48). However, at the time of the invention, it would have been obvious to a person skilled in the art that the aeronautical radio range of 108MHz – 136MHz , contains aviation communication and navigation signals, whose detection using the wideband receiver of Bexten (that has been modified based on the teachings of Mano with respect to the frequency range and channel bandwidth of interest) and is clearly of importace to an airline pilot or a traffic controller.

With respect to claims 50-52, claims 50-52 are analyzed similarly to claims 2-4 above (see 102(b) rejection under Bexten).

With respect to claim 53, Bexten discloses: at least one front-end circuit group comprising a plurality of front-end circuits (see Fig. 5, see plurality of receiving branches, where the front end circuits include elements 205, 505, 215, 510) wherein each of said front-end circuits comprises an antenna circuit (Fig. 5, element 205 is an antenna) operable to receive radio signals and an amplifier circuit operable to amplify radio signals (see Fig. 5, element 215 is a LNA also shown in Fig 2), said front-end circuits operable to receive a plurality of radio signals transmitted across a frequency band and generate an analog signal corresponding to a plurality of channels within said frequency band (each branch receives RF signals (during every uplink operation) and generates analog signal, column 4, lines 4-8); at least one analog to digital converter coupled to said at least one front-end circuit group (Fig. 5, see ADC elements), said analog to digital converter operable to receive said analog signals from said front-end circuits and convert said analog signals to a digital signal (understood to be operation of the ADC) ; and a digital processing system coupled to said at least one analog to digital converter (see Fig. 5, functional blocks, 315, 325,330, (these blocks are also present in Fig. 3) and under the control of "resource manager", see column 2, lines 56-58) , said digital processing system operable to receive said digital signal from said analog to digital converter and generate at least one output signal corresponding to at least one of said channels within said frequency band of at least one of said front-end circuits (see column 7, lines 1-2 , 26-32 , where the DSPs (elements 535 of Fig. 5) generate output signals corresponding to single carries that were included in the FDM wideband signal).

Bexten does not teach: wherein said radio signals comprise aviation navigation and aviation communication radio signals.

In the same field of endeavor, Mano discloses: radio signals comprise aviation navigation and aviation communication radio signals (see column 1, lines 50-58, wideband receiver receives radio signals from the aeronautical radio frequency range of 108-136MHz, that ins understood to include aviation navigation and aviation communication signals since these signals are considered aeronautical signals).

At the time of the invention, it would have been obvious to a person skilled in the art to configure the wideband receiver of Bexten et. al., to receive over a frequency band that comprises aviation-band radio signals (see column 1, lines 55-58, aeronautical radio spans 108MHz – 136MHz with a channel width of 25kHz) to provide a intelligent wideband receiver that centralizes, re-uses and shares system resources (see column 1, lines 50-55 of Bexten) for processing airline/aviation signals.

With respect to claim 54, all of the limitations of claim 54, are analyzed above in claim 53, and the combination of Bexten and Mano discloses: wherein said digital processing system is operable to generate a plurality of output signals (Fig. 5, TDM output generated during every uplink operation), wherein each of said output signals corresponds to at least one of said channels within said frequency band of at least one of said front-end circuits (see column 7, lines 17-20, 26-28, single carriers (channels) are processed (demodulated) by the DSPs that are contained in the spectrum (aeuronautical spectrum based on the teachings of Mano)).

With respect to claim 56, all of the limitations of claim 56 are analyzed above in claim 54, and claim 56 is analyzed similarly to claim 10 above (see 102(b) rejection under Bexten).

Method claim 57 is analyzed similarly to apparatus claim 46-48 above.

With respect to claim 58, claim 58 is analyzed similarly to claim 57 above, and with respect to: further comprising mixing said received radio signals to an intermediate frequency band (see column 4, lines 9-10 of Bexten for IF conversion).

With respect to claim 59, all of the limitations of claim 59, are analyzed above in claim 58, and Bexten disclose: wherein said output signal is generated by: applying software configurable channel selection parameters to said digital signal to select at least one of said digitized channels within said frequency band see column 7, lines 18-20, where it is mentioned that the digital receivers can be programmed to select any single channel within the FDM spectrum, and column 3, lines 18-23, where the FDM spectrum includes 416 (each one spans 30KHz), channels for a total of 12.5MHz, therefore to select any one of these 416 channels involves changing a channel (center) frequency, and also see column 1, lines 50-57, where programmable frequency bandwidths are mentioned, and column 8, lines 5-8 where the programmable receivers can accommodate different standards (GSM, AMPS, DECT, etc) ; extracting information from said at least one of

said selected digitized channels according to software configurable channel decoding parameters; ((see column 7, lines 38-46, where the number of diversity branches connected to a single DSP that demodulates (decodes) the channels, can be adjusted and also see column 7, lines 56-60 where the channel information format (voice or control signal) is determined). and conveying said extracted information within said output signal (Fig. 5, output signal T1 supplied to MSC shown in Fig. 2).

Allowable Subject Matter

11. Claims 17, 20, 55 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Graham et. al., (U.S. 5,355,141) disclose: a channelised receiver for direction finding.
Sorrells et. al., (U.S. 7,006,805) disclose: a wideband receiver that can be used over a plurality of frequency bands and channels.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SOPHIA VLAHOS whose telephone number is 571 272 5507. The examiner can normally be reached on MTWRF 8:30-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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10/29/2006


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